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Miracle Box v3.04 Setup. Revisiting the effect of time on maternal care in the intermediate phase of lactation. Maternal behavior in the intermediate phase of lactation, which occurs from the day of parturition until 5 days postpartum, is sensitive to alterations in maternal environmental conditions. We compared maternal interactions with pups between mothers experiencing long vs. short postpartum intervals with a visual probe of pup investigation. Mothers with short postpartum intervals (n=9) were allowed more time to interact with pups than mothers with long intervals (n=9), from parturition to 5 days postpartum. However, when the time interval was the same, short-term maternal behavior was observed in mothers with a short postpartum interval, irrespective of the time of birth. The current findings indicate the sensitivity of maternal care to environmental contexts and suggest that early postpartum maternal behavior might be selectively affected depending on the amount of maternal care provided during the postpartum interval. The present invention relates to a wiring structure of a semiconductor device, and more specifically to a method for manufacturing the wiring structure of a semiconductor device in which the width of the wiring portion of the wiring layer in the semiconductor device is increased and the wiring resistance is reduced. FIG. 1 is a cross sectional view for illustrating a conventional technique for manufacturing a conventional wiring structure of a semiconductor device. Referring to FIG. 1, in the conventional wiring structure of the semiconductor device, a first insulating layer 102 is formed on a substrate 100 made of silicon. An interlayer insulating layer 104 is formed on the first insulating layer 102. On the interlayer insulating layer 104, a second insulating layer 106 is formed. Then, a first wiring layer 108 is formed on the interlayer insulating layer 104. Then, a third insulating layer 110 is formed on the first wiring layer 108. A second wiring layer 112 is formed on the third insulating layer 110. The first wiring layer 108, the interlayer insulating layer 104, the second insulating layer 106, the third insulating layer 110, and the second wiring layer 112 are etched using a resist layer (not shown) as an etching mask, to form contact holes. However, in the conventional wiring structure of the semiconductor device, it is difficult to reduce the thickness of the second insulating layer 106 to a relatively small thickness, because it is necessary to reduce the thickness of the inter



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